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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,807	02/27/2004	Ming-Sheng Tung	251613-1020	7848

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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/788,807	TUNG ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed August 5, 2005.

Response to Amendment

The limitations added to claims 1 and 8 are sufficient to overcome the Zheng et al. (US 6,762,085) and Roy et al. (US 6,777,298) references.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 2, 5, 6, 8, 9, 12, 13, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Quek (US 6,924, 180).

Regarding claim 1, Quek discloses forming a gate including a gate dielectric layer (2) and a conductive layer (3) on a substrate (1), forming a liner (7/11/4) on the sidewall of the gate, performing a first-type ion implantation, using the gate and the liner as a mask to form a source/drain region (9) outside of the gate in the substrate, etching the liner to reduce a lateral thickness of the liner, and performing a second-type ion implantation using the gate and the etched liner as a mask to form a halo region (10) surrounding the source/drain region (Fig. 3-6; col. 2, ln. 61 – col. 4, ln. 65).

Regarding claims 2 and 9, Quek discloses that the conductive layer includes polysilicon (col. 3, ln. 2-20).

Regarding claims 5 and 12, Quek discloses that the first-type ions can be N-type ions and the second-type ions can be P-type ions (col. 4, ln. 15-61).

Regarding claims 6 and 13, Quek discloses that the first-type ions can be P-type ions and the second-type ions can be N-type ions (col. 5, ln. 19-32).

Regarding claim 8, Quek discloses forming a gate including a gate dielectric layer (2) and a conductive layer (3) on a substrate (1), forming a liner (7/11/4) on the sidewall of the gate, performing a first-type ion implantation, using the gate and the liner as a mask to form a source/drain region (9) outside of the gate in the substrate, etching the liner on one sidewall of the gate to reduce a lateral thickness of the liner, and performing a second-type ion implantation using the gate and etched liner as a mask to form a halo region (10) surrounding one of the source/drain regions adjacent to the etching side (Fig. 3-6; col. 2, ln. 61 – col. 4, ln. 65).

Regarding claim 16, Quek discloses forming a mask layer covering another side of the gate prior to etching the liner (col. 2, ln. 20-30; col. 5, ln. 10-30).

Regarding claim 17, Quek discloses that the mask layer is a photoresist layer (col. 2, ln. 20-30; col. 5, ln. 10-30).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 3, 7, 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quek (US 6,924,180) in view of Park et al. (US 20050048732).

Regarding claims 3 and 10, Quek does not disclose forming a silicide layer on the polysilicon layer. Like Quek, Park discloses a method of forming a transistor on a semiconductor substrate. Park discloses that it is conventional in the art to form silicide on the

gate, source and drain regions of the transistor (para. 0048). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form silicide on the gate of Quek because it is conventional in the art to silicide the top of a polysilicon gate for the purpose of decreasing its resistance.

Regarding claims 7 and 14, Quek does not disclose forming a cap layer on the gate conductive layer. Park discloses forming sacrificial cap layers on the transistor during fabrication. Park teaches that these cap layers provide the advantage of artificially increasing the gate height, thereby making it possible to perform source, drain and halo implantation at an energy high enough to sufficiently dope the source/drain and channel regions without incurring the problem of boron penetration through the poly gate and gate dielectric layer (para. 0029). At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide the gate of Quek with the cap layers of Park because Park teaches that the cap layers offer the advantage of preventing the problem of boron penetration through the gate and gate dielectric layer.

Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quek et al. (US 6,924,180) in view of Oyamatsu (US 6,734,506, previously cited).

Regarding claims 4 and 11, Quek does not disclose that the liner is formed by a rapid thermal oxidation (RTO) process. Like Quek, Oyamatsu discloses a process of forming MOSFETs for use in an integrated circuit. Oyamatsu teaches that a gate can be oxidized to form an oxide layer on the sidewall thereof, by using a rapid thermal oxidation process (col. 6, ln. 66 – col. 7, ln. 8). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the liner of Quek by using a rapid thermal oxidation process because Oyamatsu

teaches that a RTO process can successfully oxide the sidewalls of a gate to form an oxide layer thereon and because the RTO would be faster than depositing the liner using TEOS.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Quek (US 6,924,180) in view of Yu et al. (US 20030222298, previously cited).

Regarding claim 15, Quek's invention is a method of forming a MOSFET device and does not place any limits on the integrated circuits for which the MOSFETs of his invention may be used. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the MOSFETs of Quek in any integrated circuit, including that of a memory cell circuit because Quek teaches forming a MOSFET and because memory cells having MOSFET access transistors are well-known in the art. That being said, in the event that the MOSFET design of Quek is applied to the creation of a memory cell, it is conventional in the art to form a bit line connected to the source/drain region of the transistor, as is shown by Yu (Fig. 4).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
October 5, 2005

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800